

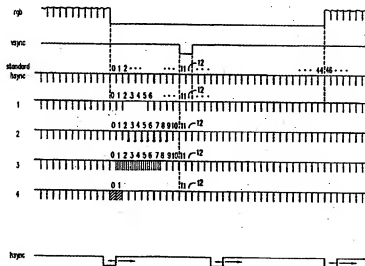
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(71) Applicant: MACROVISION CORPORATION [US/US]; 1341 Orleans Drive, Sunnyvale, CA 94089 (US).			
(72) Inventors: RYAN, John, O.; 22015 Creekside Court, Cupertino, CA 95014 (US). QUAN, Ronald; 10910 Wunderlich Drive, Cupertino, CA 95014 (US). KUROWSKI, Kordian, J.; 3673 Meadowlands Lane, San Jose, CA 95135 (US).			
(74) Agents: BRILL, Gerow et al.; Macrovision Corporation, 1341 Orleans Drive, Sunnyvale, CA 94089 (US).		Published With international search report.	

(54) Title: PROTECTION OF A COMPONENT VIDEO SIGNAL



(57) Abstract

A VGA (or other component video signal) output, e.g. from a computer or DVD player, is protected so it is viewable on a VGA monitor. However, if the component video signal is converted to composite video (e.g. television) the resulting television picture is of substantially degraded quality, thereby inhibiting viewing and/or copying. This protects for instance copyrighted material in the VGA format from unauthorized use. The protection involves modifying the horizontal or vertical synchronization signals in the VGA video in such a way that there is no adverse affect on a typical VGA monitor. However, most or all VGA to television converters and/or television sets and VCR's suffer from loss of synchronization, resulting in an unviewable picture. Also, methods and circuits for defeating the copy protection are provided.

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PROTECTION OF A COMPONENT VIDEO SIGNAL

CROSS REFERENCE TO RELATED APPLICATION

5 This application claims priority to U.S. provisional application S.N. 60/051,312, filed JUNE 30, 1997, "A VGA Copy Protection System and Method", John O. Ryan et al and U.S. Provisional 60/056,570 filed AUGUST 21, 1997, "PROTECTION OF A COMPONENT VIDEO SIGNAL".

10 Field of the Invention

This invention relates to video signal protection and more specifically to such protection for component video.

Background of the Invention

15 With the advent of the Digital Video Disc (DVD) format, manufacturers and users of personal computers are incorporating the ability to playback movies or other recorded material recorded on DVD's via the personal computer. Copy protection measures are being incorporated
20 within these computers to protect the analog (NTSC or PAL television) video output from such a device. This is being done by incorporating bits within the digital stream on the DVD to instruct a digital to analog converter and NTSC (or PAL) encoder integrated circuit to incorporate copy
25 protection pulses onto the analog video output signal. The copy protection techniques being used on the analog output include e.g. those in US patents Nos. 4,631,603; 4,819,098; 4,577,216; and US patent applications No. 08/784,876 filed January 16, 1996; and International applications
30 PCT/US96/17719, filed November 5, 1996, and PCT/US97/05095 filed March 25, 1997, all assigned to Macrovision Corporation and incorporated herein by reference.

A computer display uses a VGA (or similar or equivalent) output signal of the computer. This VGA output
35 signal ("component video") is provided on a multiwire bus that provides separately a red video signal, a green video

television monitor. Also, if an attempt is made to copy this signal for instance using a conventional NTSC/PAL VCR (video cassette recorder), the resulting recording is also unviewable. By unviewable is meant a picture exhibiting artifacts, as described above, which substantially degrade the resulting picture when displayed on the television set.

It has been found that the most advantageous modifications to the sync pulses in accordance with this invention are to modify the horizontal sync pulse in the first part of the vertical blanking interval, e.g. prior to the occurrence of the vertical sync pulse. This typically means in the first 10 lines of the vertical blanking interval (VBI). Also, it has been found that in general it is undesirable to have a net increase in the total number of horizontal sync pulses in the VBI in any one video frame since this tends to adversely affect some VGA monitors.

Hence in one embodiment, one or more horizontal sync pulses are deleted from the first part of the vertical blanking interval. For increased effectiveness of the copy protection, one horizontal sync pulse is added, but in a place where such a horizontal sync pulse is not normally present, e.g. in the middle of a particular horizontal video line. The pattern by which horizontal sync pulses are deleted and/or added may be the same in every frame, or may vary from frame-to-frame. If it varies, the variation may be a fixed pattern, a pseudo-randomly varying pattern, or a randomly varying pattern. The varying patterns have been found to increase copy protection effectiveness. In another embodiment, the number of horizontal sync pulses is increased by adding several horizontal sync pulses to each line, for instance in the first portion of the vertical blanking interval. As mentioned above, with some VGA monitors, this degrades playability.

Other patterns for removal and/or addition of horizontal sync pulses are also possible.

Also in accordance with other embodiment, the vertical sync signal is altered, but this has been found to affect some VGA monitors adversely.

Also in accordance with the invention, a particular
5 modification pattern to the sync pulses is dependent upon the characteristics of the attached VGA monitor. This is possible because in the computer environment, it is possible for the computer to "know" the characteristics of the attached VGA monitor as supplied by the user. In this case,
10 the particular modification pattern may be set adaptively to accommodate the particular VGA monitor so as to minimize adverse affects on playability. Also, the present VGA copy protection scheme may be turned on or off either by content present in the source video material, e.g. on the DVD, or
15 otherwise. This turning on and off may be either only to protect certain (copyrighted) material or may be done to increase the effectiveness of the anti-copy protection scheme by periodically switching between different versions of the process and/or by turning it on and off, thus further
20 confusing any VGA to NTSC/PAL converter.

It should be noted that while some VGA to NTSC converters will produce a static response to a particular version of the present protection signal, a majority of converters exhibit picture tear dynamically or produce non-
25 copiable results.

This static response to the protection signal may be in the form of a static picture shift and or static brightness change and/or static distortion (i.e. tear) in the picture when the output of the converter is connected to the TV set
30 or VCR. However, this static response would be still copiable and viewable on a VCR and TV set. Therefore, to increase the annoyance factor, the particular protection signal may be turned off for a short time in a periodic or random fashion. By turning off the protection from time to
35 time, the output of converter will have a dynamically shifted picture and/or dynamically distorted picture when

connected to a TV set and/or VCR. This causes a more effective protection signal when the converter is connected to a VCR (and also a less viewable picture on the TV set).

5 Of course, it may be even more effective to affect a greater population of converters by alternating different protection processes in accordance with the invention along with turning off the protection from time to time.

While the references here to television typically are in terms of NTSC/PAL, other television standards, e.g. SECAM
10 would also be vulnerable to the present modifications.

Also, circuitry is disclosed herein for suitably modifying the VGA video signal so that it contains the protection modifications. While several such embodiments are disclosed, it is to be understood that these are not
15 limiting and a wide variety of other circuits would provide the desired modifications. Moreover, the circuits described herein only provide certain types of modifications, whereas a greater range of modifications is disclosed herein. It would be well within the skill of one of ordinary skill in
20 the art to design and build circuitry to carry out the other types of modifications disclosed herein.

For example, the horizontal sync pulse modifications need not be restricted to the vertical blanking interval. Horizontal sync pulse train deletions and/or additions can
25 be in the vicinity of the vertical blanking interval or anywhere in the field including in the active field. In some cases the horizontal sync pulse train is modified anywhere in the field by horizontal sync pulse splitting, pulse width modulation and the like. Also, vertical sync
30 pulse train modifications can be made by adding pulses in the vertical sync pulse train. Other vertical sync pulse train modifications may include vertical sync pulse width modulation and/or splitting.

Because it is possible for the computer to be informed
35 (or set by the user) as to which monitor is connected thereto, maximum copy protection effectiveness for VGA type

converter boxes can be achieved with yet an additional copy protection signal. For instance, in certain monitors, the video clamp pulse may be coincident to the first 70% of the horizontal blanking interval of the red, green and blue video channels. Therefore, an additional copy protection method modifies the video channels with peak white pulses during the last 30% of the horizontal blanking interval.

Therefore in some cases an anticopy signal is inserted into at least a portion of the horizontal blanking interval (or in the vicinity of the horizontal blanking interval) over a sufficient number of lines of the component video signal (i.e. any combination of red, green, and/or blue). This anticopy signal may be an "AGC" pulse as described in U.S. Patent No. 4,631,603, referred to above. Also, this anticopy signal can be a static and/or periodic and/or random and/or pseudo-random signal of various amplitudes and/or frequencies and/or phases and/or positions and/or widths.

Also, while the particular illustrated circuitry for providing these modifications is shown as isolated circuits, these circuits may be incorporated for instance on an integrated circuit which includes other functionality and which is installed in the computer which hosts the DVD player, or otherwise connected thereto. It is to be expected that in one commercial embodiment, the present circuitry is included in an integrated circuit associated with the DVD player and which performs other functions for controlling the DVD player and/or its output.

Additionally, a method of defeating such a protection scheme is disclosed herein, to protect the users of the protection (e.g. copyright owners) from unlicensed individuals that make, use and sell so called "defeat" devices. A similar pattern of copy protection technologies and corresponding defeat devices are known in the analog video copy protection technologies referred to above.

Therefore an associated protection defeat method and apparatus includes inputting the modified synchronizing pulses to a synchronizing generator that uses one or more of the modified pulse trains to generate a proper horizontal and vertical synchronizing pulse train. This proper pulse train when connected to a VGA to NTSC/PAL converter produces copiable NTSC/PAL video signals.

BRIEF DESCRIPTIONS OF THE DRAWINGS

Figure 1 shows the normal RGB and horizontal and vertical synchronizing signals of a VGA output signal of a computer.

Figures 2A to 2C show the same signals as Figure 1.

Figures 2D to 2H show waveforms for four copy protection methods in accordance with the invention.

Figures 3 and 4 show high level block diagrams of how copy protection is applied in accordance with this invention.

Figures 5 and 6 show detail of Figures 3 and 4.

Figure 7A, 7B show a copy protection defeat method and an associated diagram of a copy protection defeat circuit.

Figures 8, 9, 10, and 11 show diagrams of other copy protection defeat circuits.

DETAILED DESCRIPTION

As discussed above, the present protection of VGA (including SVGA or other component video output) comprises a modification of at least one of the synchronizing signals in the VGA output signal from e.g. a computer. The goal is to modify one or both of the sync pulse trains to cause a VGA to NTSC (or PAL) converter to allow a recording that is totally lacking in entertainment value, without affecting the VGA display on the VGA computer monitor.

The following are distinguishing characteristics between such converters used in combination with TV sets/monitors and computer monitors pertinent to their

horizontal scan (synchronization) circuits exploited in accordance with the invention.

1) In TV sets, the horizontal scans are driven by a fly-wheel oscillator (horizontal phase lock loop oscillator with relatively slow AFC response) that is immune to noise in the horizontal sync line.

2) In a computer monitor, the horizontal scan circuit does not always have flywheel circuits to reject noise as in TV sets. Instead, the computer monitor triggers an oscillator off an edge of the horizontal sync pulse. Triggered oscillators react almost instantaneously to even narrow pulse width noise spikes in the horizontal sync pulse train. There are some computer monitors that have flywheel oscillators but with much faster locking than TV sets. That is, the horizontal AFC (automatic frequency control) loop is slower in a TV set than in a computer monitor.

Since different VGA to NTSC/PAL converters are affected differently by different configurations of pulse modifications, another embodiment is to vary the implementation of the horizontal sync pulse train modifications over one or more frames to include combinations of the modifications so as to produce unviewable outputs of the VGA to NTSC/PAL converter on the entire population of known converters.

As discussed above, one application of the invention disclosed here is to provide a copy protected output of copyrighted material from DVD's. The individual DVD's already have "trigger bits" associated with their normal analog output signal. These trigger bits indicate to the copy protection circuit for the analog output of the computing device that the DVD is copy protected and should have the analog copy protection signals added.

These copy protection trigger bits can also be used in accordance with the invention to indicate to the present VGA output system to modify the sync pulse trains. When the user is viewing material that does not contain trigger bits,

he is thus able to use a VGA to NTSC/PAL converter to make copies. It is only when such trigger bits indicating copy protected material are present that the VGA copy protection is activated.

5 Figure 1 shows three waveforms that together represent one of the VGA standards, the 640 by 480, noninterlaced, 60 frames-per-second format. The top line is the vertical sync pulse. It is to be understood that these wave forms are only for a portion of one frame but show the entire vertical
10 blanking interval (VBI) and a small portion of the frame prior to and subsequent to the VBI. As shown, in VGA the vertical sync train is one vertical sync pulse per VBI. With reference to the next waveform which is the corresponding horizontal sync pulses, with the horizontal
15 lines numbered, the vertical sync pulse occurs between lines 11 and 13 of the VBI. In this case, the horizontal sync signals are shown as very narrow pulses. In actuality, they have a certain width, typically 3.77 microseconds. The vertical sync pulse is two lines wide and hence has a width
20 of 63.5 microseconds. (This is for VGA having 525 lines per frame with a 60 frame per second refresh rate where 480 of the frames are active video; the remaining lines are in the VBI.) It is also to be understood that one NTSC horizontal scan line period corresponds to two VGA horizontal scan line
25 periods.

The third waveform in Figure 1 is the RGB signals, all three of which are shown combined since for the purposes of this invention there is no need to discuss each color separately. This shows the active video which of course has
30 the "black" value during the period of the vertical blanking interval. The variations in the RGB signals indicate active video. Also, as shown, during the period of the horizontal sync signal, the RGB signals go down to the black level. It is to be understood that the RGB, horizontal sync and
35 vertical sync signals shown in Figure 1 do not include copy protection in accordance with this invention, but are shown

for purposes of reference to those not familiar with the VGA format. As is conventional, the horizontal axis represents time and the vertical axis represents signal amplitude in terms of voltage.

5 Protection in accordance with this invention is understood with reference to Figures 2A-2G. Figure 2A is the same as the RGB waveform in Figure 1; Figure 2B is the same as the vertical sync waveform in Figure 1; Figure 2C is the same as the horizontal sync waveform in Figure 1.

10 Figure 2A-2C are for purposes of illustration to show which portions of the video signal are illustrated in Figures 2D-2G.

Figures 2D-2H illustrate five embodiments of a protection method in accordance with this invention in terms of the VGA waveforms output by the protection circuitry. These protection modifications all occur during the vertical blanking interval and, in fact, occur prior to the vertical sync signal, in the first 10 lines of the vertical blanking interval. This particular form of protection has been found to maximize playability (have the least affect on the universe of known VGA monitors), while providing relatively effective protection as described above. In Figures 2C-2G the horizontal lines are numbered so that the first line in the VBI is line 0 and the vertical sync signal occurs from lines 11 to 12 of the frame. The vertical blanking interval terminates at line 45 of the frame.

Figure 2D shows a first protection method in accordance with this invention. In this case in this frame, three horizontal sync pulses are deleted, at lines 3, 4, and 5.

10 In the second method, shown in Figure 2E, one horizontal sync pulse is deleted in each frame. As shown by the wiggly lines, this is not the same horizontal sync pulse in every frame; instead, the particular single horizontal sync pulse deleted from each frame varies from frame to frame, and can be in any one of lines 3-9. This frame to

frame variation may be, for instance, random or pseudo random or follow some particular fixed pattern.

The third method, shown in Figure 2F, does not delete horizontal sync pulses but instead adds them, so that each particular horizontal line includes, in addition to the normal single horizontal sync pulse at the beginning of the line, for instance three extra horizontal sync pulses inserted during the remainder of the line during, in this case, each of lines 1-7. This increased density of

horizontal sync pulses for instance might be the same for every frame or may vary frame-to-frame, and need not be present in each frame. This causes playability problems on some monitors as described above. Adding some sync pulses therefore is compensated for by subtracting some others. Therefore, this method works best in conjunction with either the first or the second method described above.

The fourth method, shown in Figure 2G, adds one horizontal sync pulse at a location varying between lines 0 and 1. The added horizontal sync pulse is added e.g. in the middle of the line. The line at which the horizontal sync pulse is added may vary from frame to frame either in a fixed pattern or randomly or pseudo randomly.

The fifth method, shown in Figure 2H, pulse-width modulates the horizontal sync pulses in the VBI. (Figure 2H is not to the same scale as Figures 2A to 2G.) The horizontal sync pulse widths may vary between two or more individual discrete values at any frequency ranging from 1 sync pulse width change per several frames to 1 sync pulse width change per line. The sync pulse width may be altered by keeping the pulses leading edge in the standard location and moving the pulse trailing edge. Note that the location of the entire horizontal sync pulse may be varied, by varying the location of both the trailing and leading edges. Not all horizontal sync pulses in the VBI need be so modulated. A compromise between playability and effectiveness has been found to jump between the standard

pulse width and 5 to 10% wider than standard every several frames. Also, sync pulse width modulation may be applied only to a group of selected lines, such as only during the VBI.

5 Alternately the vertical sync pulses may be delayed or advanced by a sync pulse width or fraction thereof. Another modification is to add narrow width positive-going pulses inside particular horizontal sync pulses.

10 Turning the modifications on/off every few frames, combining several of these methods simultaneously, and switching between different methods every few frames is possible and some combinations of this type been found to increase copy protection effectiveness with various converters.

15 It is to be understood that these methods are only illustrative and various modifications and combinations of these methods are also contemplated within the scope of the invention. However, these particular patterns have been found to maximize copy protection effectiveness while
20 minimizing playability problems across various commercially available VGA to NTSC to PAL converters and VGA monitors.

As noted above, the presently disclosed anticopy protection scheme need not be identical frame-to-frame. For instance, the deletion of the horizontal sync pulses may
25 vary from frame-to-frame in terms of the number and location. The same is true of adding horizontal sync signals as in Figure 2G. In another variation, horizontal sync signals are both added and subtracted. For instance, one horizontal sync pulse may be deleted at a random
30 location and another one added at a different location, e.g. in the middle of a line. One embodiment is to delete one horizontal sync pulse in one portion of the horizontal sync pulse train and add a horizontal sync pulse at a different portion of the horizontal sync pulse train in each VBI. In
35 another embodiment, one horizontal sync pulse is deleted and two horizontal sync pulses are added per VBI.

It has been found generally as discussed above that is undesirable for playability purposes to add one or more horizontal sync pulses over the normal number per frame without deleting a corresponding number or greater somewhere else in the frame. In this case, the Figure 2F embodiment may be problematic with certain VGA monitors.

One variation that has been found to be particularly effective and provide good playability involves the combination of the Figure 2E and Figure 2G methods. That is, a horizontal sync signal is deleted from either the 0 or first line as shown in Figure 2G and a horizontal sync signal is added, e.g. in the middle of the line, in for instance line 8 as in Figure 2E. The variation between the deletion in lines 0 and 1 is varied frame-to-frame so that there are three states; the first state there is no deletion, in the second state, the horizontal sync is deleted from line 0; and in the third state, the horizontal sync is deleted from line 1. The state variation frame-to-frame may again be either a fixed pattern, randomly or pseudo randomly frame-to-frame. The above-described fifth method may be superimposed onto this composite method to increase effectiveness.

Figures 3-6 illustrate one embodiment of circuitry for carrying out protection in accordance with this invention. Figure 3 is a high level block diagram showing the relevant computer and video components. In a typical example, all of the elements shown in Figure 3 are incorporated within the housing of a personal computer, although this is not limiting.

Of course, only the relevant portions of the personal computer are shown for purposes of simplicity. The conventional DVD player 60 plays a conventional DVD. This player 60 is shown pictorially as a disc. The present invention is not limited to output from a DVD player, but in fact is applicable to all VGA output signals. However, it

is contemplated that a typical commercial embodiment is to copy protect copyrighted material provided on a DVD.

The signal output by the DVD player 60 is coupled via a conventional bus 62 to an MPEG2 decompressor 64 which is typically a card installed in the personal computer and is of a commercially available type. Decompressor 64 outputs component video on a bus 68. Moreover, the decompressor 64 outputs an "ACP on" signal on line 70, and on line (e.g. coaxial cable) 72 outputs an NTSC/PAL analog video signal for connection to a television set or VCR. ("ACP" refers to anti-copy protection", the same as copy protection.) As described above, typically this NTSC or PAL analog video signal is copy protected in the analog domain by the above-described well known copy protection methodology.

The component video on bus 68 and the "ACP on" signal are coupled into a VGA card 90. VGA card 90 includes conventional VGA processing circuitry which converts the component video into the desired VGA format and is a commercially type of product. The VGA card 90 together with the VGA ACP (anticopy protection) processor 92 together may be integrated into a single card 86 or otherwise interconnected as shown. The VGA card 90 outputs on bus 94 the VGA video to the VGA ACP processor 92 which is the novel element shown in Figure 3 in accordance with this invention.

The "ACP on" signal on line 70 is similarly coupled to the VGA ACP processor 92. In this case, in order for a user to connect to the output signal of the VGA card 90 an external NTSC/PAL device which is a VGA to NTSC/PAL converter, the user must couple the external device to the VGA output bus 98.

Of course, if the user were to tap into the bus 94, he could bypass the VGA ACP processor completely and thus bypass the present protection process. It is anticipated that the typical user will not do this. Moreover, if the VGA card 90 and the VGA ACP processor 92 for instance are incorporated together on a single integrated circuit chip,

such tapping would be rendered virtually impossible, especially since the intermediate bus 94 can be omitted. In this case, a protected signal is generated to begin with in the VGA card 90 and the standard VGA signal never exists in this implementation.

The signal on the ACP on line 70 turns the VGA ACP processor 92 on. The absence of such signal on line 70 turns the processor 92 off and no protection is provided. Hence, the material on the DVD being played on player 60 determines whether the anticopy protection in accordance with this invention is applied or not. The protection may be selectively turned on and off depending on the video material.

Figure 4 shows a more detailed view of selected elements of Figure 3, including the PC card 86, the VGA card 90, and the VGA ACP processor 92. As shown, the bus 94 in Figure 3 includes bus 102 which carries the RGB three component video, as well as a vertical sync line 104 and a horizontal sync line 96. Together these comprise the VGA video, with additional conventional lines which include various ground lines etc. and are not shown for simplicity. As shown, the lines 102 and 104 bypass the VGA ACP processor 92 in this embodiment. A jumper is available shown so that the vertical sync line 104 may be altered by processor 92 if desired. However, since the typical embodiments disclosed herein modify the horizontal sync pulses, in this case only the horizontal sync signal on line 102 is actually modified by the processor 92.

The output signals from the PC card 86 are provided on a VGA connector 98 which is coupled via a bus 110 to a NTSC/PAL converter. Converter 112 is typically a personal computer to NTSC/PAL television converter usually of the type commercially available. These are typical after market devices and as shown are not a portion of the computer, although of course they could be incorporated in the computer as a card. As shown, the output signals from the

converter 112 are provided on a line 118 to a conventional television set or monitor 120. The VGA output signal is also connected directly (if desired) to the standard VGA monitor 126 by bus 122. As shown, the connection to the
5 converter 112 and the monitor 126 is selective, depending on which device is plugged into the VGA output port 98.

The present protection process is provided by the processor 92 shown in greater detail in Figure 5. Elements in Figure 5 similar to those in the other figures are
10 identically labeled. The input signals to the ACP processor 92 include the vertical sync pulses on line 104 and the horizontal sync pulses on line 96.

Counter 130 counts the input horizontal sync pulses on line 96 and pseudo-randomly outputs an output labeled RND.
15 Line counter 132 receives a horizontal sync pulses on line 96 as well as the vertical sync signal on line 104 which acts as a counter reset. The horizontal sync pulses on line 96 are counted by line counter 132 as described, in further detail below. The output signals from line counter 132 are
20 a signal "delete hsync" on one line indicating deletion of horizontal sync and a signal "add hsync" on another line indicating addition of horizontal sync.

The third main element in Figure 5 is a half line delay
25 138 also driven by the horizontal sync pulses on line 96 as inverted by inverter 136. This provides a one-half line delay of the inverted horizontal sync pulses on the output line "delayed hsync". As shown, the four output signals from elements 130, 132 and 138 are combined by logic gates
30 140 through 160 to provide a horizontal sync signal "hsync out" on line 102. This is a modified horizontal sync pulse train and in effect replaces the original horizontal sync pulse train on line 96.

This particular circuit therefore has a facility for deleting horizontal sync pulses and adding horizontal sync
35 pulses. The added pulses are added in the middle of a line, hence the half line delay 138. Figure 5 is better

understood with reference to Figure 6 which shows the detail of line counter 132. The horizontal sync signal in on line 96 clocks a 480 line counter 170 which counts from 1 to 480 and outputs a 9-bit (digital) output signal indicating the line count. This output signal is applied to the a input terminals of three comparators 174, 176 and 180. As shown, the b input terminal of each of the comparators 174, 176, 180 is respectively connected, either programmably or hardwired, to a digital value respectively of 4, 1 and 2.

10 The output signal from the comparator 174 is the delete hsync signal also shown in Figure 5, while the outputs of comparators 176 and 180 are combined by the OR gate 184 to provide the add sync signal. Since the add sync signal in Figure 5 is modified by the random signal and, the effect is
15 that a horizontal sync pulse is pseudo-randomly added, its location varying with each frame so that there are three states; in the first state no horizontal pulse is added, in the second state it is added on line 1 in the VBI, and in the third state it is added on line 2 of the VBI. The value
20 4 input to comparator 174 indicates that the horizontal sync pulse in this case is deleted on line 4. Of course each of these values (4, 12) can vary by varying the location of the deletion/addition. Hence Figures 5 and 6 are merely illustrative of one embodiment of a copy protection circuit
25 in accordance with this invention.

As indicated above, in addition to the method and apparatus for VGA protection, the present inventors have discovered a method and apparatus for defeating their protection system. This is analogous to the defeat approach
30 to defeat the analog copy protection described above; examples of such defeat approaches for analog video are shown in U.S. Patent Nos. 5,194,965, 4,695,001, and 5,633,927, incorporated herein by reference. One present defeat method is to couple between the modified VGA signal
35 output from processor 92 and the input to converter 112 a circuit that inputs the modified sync pulse trains to

trigger a pulse generator to produce pulse trains not containing any of the deleted or added lines.

One such defeat method is shown, in terms of waveforms, in Figure 7A. This illustrates detecting the leading (negative) edge of the vertical sync pulse (top waveform) in each frame, giving a pulse at this leading negative edge (second waveform). This once per frame pulse is used to generate a series of pulses at the correct horizontal line rate (third waveform) which in turn trigger regenerated horizontal sync pulses of the correct length at the correct locations (fourth waveform).

The associated defeat circuit is shown in Figure 7B. The protected (modified) VGA video is coupled to RGB port 190 and lines 192, 194. The input vertical sync pulse train on line 192 (which is not modified) triggers negative edge detector 198 to output the vertical negative edge pulse on line 199 which drives a divide by 525 phase lock loop 200. In this case, there are 525 lines per frame. PLL 200 outputs the line rate pulses of Fig. 7A (third waveform) on line 204 to drive a 3.77 microsecond duration one shot 206 which outputs, after inversion by inverter 210, the regenerated (correct) horizontal sync pulse train (fourth waveform of Figure 7A) on line 212.

The circuit of Figure 8 defeats the present VGA protection by using a fly-wheel filter to ignore added pulses in the horizontal sync train and also to fill in missing horizontal sync pulses. The vertical sync pulse train is optionally filtered if noise signals are present as part of the protection scheme.

With reference to Figure 8, the horizontal sync pulse train is regenerated such that normal horizontal sync pulses are reestablished. This is done by first filtering out any noise signals in the input horizontal sync (hsync) with H LPF 220, a low pass filter that passes through horizontal sync pulses. The output signal from low pass filter 220 then is coupled to the trigger input at a one shot circuit

222 (OS1) that is non-retriggerable. This one shot 222 outputs a pulse that is about 90% to 99% (30 μ sec) the duration of a horizontal pulse period, so that any further noise or protection signals in the active portion of the horizontal sync pulse train are ignored. The output signal of one shot 222 then is running at horizontal rate, except whenever a horizontal sync pulse deletion caused by the protection occurs. The output of one shot 222 then is shaped (optionally) by one shot 226 (OS2) which generates about a 50% duty cycle horizontal rate pulse (16 μ sec duration).

The output of one shot 226 then is filtered via a bandpass filter/amplifier 228 of high Q such that ringing occurs with an impulse or step signal, providing dropout compensation. The amplified output is coupled to a phase shifter 232 to match the phase of the input horizontal sync pulses. The output of the phase shifter 232 is then translated to logic levels by slicer 234 and then coupled to one shot 238 (OS3) to set the pulse duration of the new regenerated horizontal sync pulses at their nominal value, free of protection due to deleted or added sync pulses. As shown, the vertical sync pulses are optionally subject to vertical low pass filter 240.

If noise is present or modifications are done to the vertical sync pulses, the modified vertical sync pulses can be made free of copy protection by using the same type of method as described above for horizontal sync pulses. That is, one uses a fly-wheel filter tuned to vertical rate to regenerate the copy protected vertical syncs.

Figure 9 shows a circuit for removing the added or deleted signals (i.e. sync pulses) for the horizontal and/or the vertical sync pulse trains by using respectively phase lock loop circuits 244, 248 to defeat the copy protection signals. The respective one shot circuits 250 (OS4) and 252 (OS5) define corresponding output pulse widths respectively.

Figure 10 shows yet another fly-wheel circuit to remove the protection. Instead of using phase lock loop circuits, lock oscillators are used. These lock oscillators can be triggered oscillators for example. The lowpass filter 260 (LPF6) and 262 (LPF7) remove some of the noise that may be present in respectively the horizontal and vertical sync pulse trains. One shot circuits 264 (OS6) and 266 OS9 are non-retriggerable one shots with a duration of 90% to 99% of the horizontal and vertical sync pulse periods respectively. Thus, one shot 264 and one shot 266 reject noise or protection pulses in the horizontal and vertical sync pulse trains coincident with the active video. One shots 270 (OS7) and 272 (OS10) shape the pulses output by one shots 264, 266 respectively and allow the horizontal lock (H lock) and vertical lock (V lock) oscillators 276, 278 to synchronize with the incoming sync pulses. One shots 280 (OS8) and 282 (OS11) set pulse widths consistent with nominal horizontal and vertical sync pulses that are free of copy protection.

Figure 11 shows another circuit to defeat the protection by detecting the added sync pulses and the missing sync pulses. Once the missing sync pulse periods are identified, a new sync pulse is re-inserted or added back to the horizontal sync pulse train. If spurious sync signals are found, then the horizontal sync pulse train containing these will be modified such that these spurious horizontal sync pulses are narrowed attenuated, level shifted, or any combination of such that the spurious horizontal signals are not detected by the VGA (or equivalent) converter.

In the defeat circuit of Figure 11, the protected horizontal sync pulse train is input to a horizontal sync regeneration circuit 290 (as described above) which outputs standard horizontal sync pulses. The regeneration circuit 290 can be a circuit such as in Figure 8 or equivalent. The output signal of regeneration circuit 290 is input to one

input terminal of an XOR (exclusive OR) gate 292. The output signal of XOR gate 292 turns high when there is a missing (deleted) horizontal sync pulse and also turns high when spurious sync pulses (added horizontal sync pulses) are present. To identify or sense missing horizontal sync pulses, the output signal of the XOR gate 292 is coupled to an input terminal of AND gate 294 (AND2), whose other input terminal is coupled to the inverted regenerated horizontal synchronization signal via inverter 296.

The output signal of AND gate 294 is high when deleted horizontal sync pulses occur. To identify (sense) the added (spurious) horizontal sync pulses of the copy protected signal, the output signal of XOR gate 292 is connected to an input terminal of AND gate 298 (AND1). The other input terminal of AND gate 298 is coupled to the output signal of the regeneration circuit 290. Since the output signal of the regeneration circuit 290 is low during the horizontal sync pulse tips, the output signal of AND gate 298 can be high only during the times outside the interval of the horizontal sync pulses. It turns out that the added or spurious horizontal sync pulses occur in the interval outside the normal horizontal sync pulses. Therefore, the output signal of AND gate 298 is logic high during the interval of added horizontal sync pulses.

To defeat the copy protection signal, the output signal of AND gate 294 is combined (i.e. logically OR'd) with the horizontal sync pulse train to add back in the missing horizontal sync pulses. To defeat the added (spurious) horizontal sync pulses, the combining circuit 300 uses the output signal of AND gate 298 to do any or combination of the following:

a) Narrow the pulse width of the spurious horizontal sync pulses such that the protection is defeated.

b) Level shift at least a sufficient portion of the added horizontal sync pulses relative to the horizontal sync pulses such that the protection signal is defeated.

c) Attenuate at least a sufficient portion (includes elimination of the added pulses) of the added horizontal sync pulses relative to the normal horizontal sync pulses such that the protection signal is defeated.

- 5 d) Any combination of the above a, b, and/or c. Thus, the output signal of the combining circuit 300 then is the horizontal sync pulse train ("New H") free of the protection signal.

If the vertical sync signal, V sync, has protection modifications, it too can be defeated similarly as described above for the horizontal sync pulses. Otherwise, the vertical sync pulses and video signals R, G, and B are sent to the output substantially unchanged.

On the other hand, if the horizontal blanking intervals of the video channels (i.e. red, green and blue or R, G, and B) contain the anticopy signals, then defeating can be done by any of the following:

a) Replacing and/or attenuating a sufficient portion of the protection signal in or near the horizontal blanking interval over a sufficient number of horizontal lines in the video channels with a new signal such as a blanking level voltage.

b) Level shifting a sufficient portion of the protection signal over a sufficient number of horizontal lines; for example, level shifting a peak white copy protection signal down to blanking level.

c) Narrowing or increasing the frequency of the protection signal (to lower its energy) sufficiently such that the computer monitor's clamp pulse will not respond to the resultant lower energy protection signals.

d) any combinations of the above a to c.

The above description is illustrative and not limiting; other modification in accordance with the invention will be apparent to one of ordinary skill in the art in the light of this disclosure and are intended to fall with the scope of the appended claims.

We Claim:

1. A method of protecting a component video signal from unauthorized use, comprising the steps of:

modifying a synchronization signal of the

5 component video signal by adding or deleting synchronization pulses in the component video signal;

wherein the modified component video signal when played on a component video monitor produces a normal image, and the modified component video signal when
10 converted to a composite video signal produces an image having degraded viewing characteristics.

2. The method of Claim 1, wherein the component video signal is one of a VGA, SVGA, IBM XGA or other computer
15 video signal.

3. The method of Claim 1, wherein the composite video signal is one of an NSTC, SECAM, or PAL video signal.

20 4. The method of Claim 1, wherein the step of modifying comprises adding or deleting at least one horizontal synchronization pulse of at least particular frames of the component video signal.

25 5. The method of Claim 4, wherein the adding or deleting is at a location between the first horizontal line of the vertical blanking interval and the vertical sync pulse of each of the particular frames.

30 6. The method of Claim 4, wherein at least one horizontal synchronization pulse is added at a first location and at least one horizontal synchronization pulse is deleted from a second location.

7. The method of Claim 4, wherein the added horizontal synchronization pulse is added at a location other than the beginning of a horizontal scan line.

5 8. The method of Claim 4, further comprising the step of varying a position of the horizontal synchronization pulse which is added or deleted from frame-to-frame.

10 9. The method of Claim 8, wherein the varying is random.

10. The method of Claim 8, wherein the varying is pseudo random.

15 11. The method of Claim 8, wherein the varying is in a fixed pattern from frame to frame.

20 12. The method of Claim 1, wherein the step of modifying comprises adding a plurality of closely spaced horizontal synchronization pulses.

13. The method of Claim 1, further comprising the steps of:

25 prior to the step of modifying, determining if a copy protection trigger signal is present in the component video signal; and

only performing the step of modifying if the trigger signal is determined to be present.

30 14. The method of Claim 1, further comprising the step of:

both deleting and adding horizontal synchronization pulses in each frame.

35 15. The method of Claim 1, further comprising the steps of:

determining characteristics of the component video monitor; and

adaptively modifying the synchronization signal, dependent on the determined characteristics, to ensure production of the normal image.

16. The method of Claim 1, wherein the step of modifying comprises pulse-width modulating a plurality of horizontal synchronization pulses.

17. The method of Claim 1, further comprising the steps of periodically stopping the step of modifying.

18. The method of Claim 1, wherein the step of modifying includes periodically switching between differing versions of the method.

19. The method of Claim 1, wherein the added pulses are in a horizontal blanking interval of the component video signal.

20. The method of Claim 1, wherein the added or deleted pulses are in a vertical blanking interval of the component video signal.

21. An apparatus for protecting a component video signal from unauthorized use, comprising:

a circuit having two input terminals for receiving respectively a vertical synchronization signal and a horizontal synchronization signal of the component video signal, and outputting a modified vertical or horizontal synchronization signal that when supplied to a component video monitor produces a normal image, and when converted to a composite video signal produces a image having degraded viewing characteristics.

22. The apparatus of Claim 21, wherein the component video signal is one of a VGA, SVGA, IBM XGA, or other computer-type video signal.

5 23. The apparatus of Claim 21, wherein the composite video signal is one of an NSTC, SECAM, or PAL video signal.

24. The apparatus of Claim 21, wherein the circuit modifies the video signal by adding or deleting at least one
10 horizontal synchronization pulse in the vertical blanking interval of at least particular frames of the component video signal.

25. The apparatus of Claim 24, wherein the adding or
15 deleting is at a location between the first horizontal line of the vertical blanking interval and the vertical sync pulse of each of the particular frames.

26. The apparatus of Claim 24, wherein at least one
20 horizontal synchronization pulse is added at a first location and at least one horizontal synchronization pulse is deleted from a second location.

27. The apparatus of Claim 24, wherein the added
25 horizontal synchronization pulse is added at a location other than the beginning of a horizontal scan line.

28. The apparatus of Claim 24, wherein the circuit varies a position of the horizontal synchronization pulse
30 which is added or deleted from frame to frame.

29. The apparatus of Claim 28, wherein the varying is random.

35 30. The apparatus of Claim 28, wherein the varying is pseudo random.

31. The apparatus of Claim 28, wherein the varying is in a fixed pattern from frame to frame.

5 32. The apparatus of Claim 21, wherein the circuit adds a plurality of closely spaced horizontal synchronization pulses.

33. The apparatus of Claim 21, wherein the apparatus
10 further comprises:
means for determining if a copy protection trigger signal is present in the component video signal.

34. The apparatus of Claim 21, wherein the circuit
15 adds and deletes horizontal synchronization pulses in one frame of the component video signal.

35. The apparatus of Claim 21, wherein the circuit pulse-width modulates horizontal synchronization pulses in
20 the composite video signal.

36. The apparatus of Claim 21, further comprising:
means for determining characteristics of the component video monitor; and
25 means for adaptively modifying the synchronization signal, dependent on the determined characteristics, to ensure production of the normal image.

37. The apparatus of Claim 24, wherein the circuit
30 includes:

a line counter coupled to be reset by vertical synchronization pulses in the input vertical synchronization signal, and counting the horizontal synchronization pulses in the horizontal
35 synchronization signal;

a sequence counter coupled to count the horizontal synchronization pulses;

a half-line delay coupled to receive the horizontal synchronization pulses; and

5 a logic circuit coupled to receive output signals from each of the line counter, sequence counter, and half-line delay and outputting the modified horizontal synchronization signal.

10 38. The apparatus of Claim 24, wherein the circuit is periodically turned off.

39. The apparatus of Claim 24, wherein the circuit periodically switches between different versions of the
15 modified synchronization signal.

40. The apparatus of Claim 24, wherein the modified synchronization signal is in a horizontal blanking interval of the component video signal.

20 41. The apparatus of Claim 24, wherein the modified synchronization signal is in a vertical blanking interval of the component video signal.

25 42. A method of defeating a component video protection signal which modifies a synchronization signal of the component video, to inhibit conversion thereof to composite video comprising the steps of:

30 receiving the modified synchronization signal;
regenerating the modified synchronization signal to reduce the effect of the modifications;
outputting the regenerated synchronization; and
converting the regenerated synchronization signal to a portion of a composite video signal, thereby
35 providing a viewable composite video signal.

43. The method of Claim 42, wherein the step of regenerating comprises:

generating a normal horizontal synchronization signal from a vertical synchronization signal in the component video signal; and

outputting the normal horizontal synchronization signal.

44. The method of Claim 43, wherein the step of generating comprises:

detecting an edge of a vertical synchronization pulse in the vertical synchronization signal;

generating a series of pulses at a horizontal line rate in response to the detected edge; and

using the generated series of pulses each to generate one horizontal synchronization pulse.

45. The method of Claim 42, wherein the step of regenerating includes:

removing any added horizontal synchronization pulses in the modified synchronization signal; and

generating a ringing signal to add a horizontal synchronization pulses to the modified synchronization signal.

46. The method of Claim 42, wherein the step of regenerating includes:

removing any added synchronization pulses in the modified synchronization signal; and

driving an oscillator with the synchronization signal to generate synchronization pulses added to the synchronization signal.

47. The method of Claim 42, wherein the step of regenerating comprises:

driving a phase lock loop with the modified
synchronization signal; and
using an output signal of the phase lock loop to
generate normal synchronization pulses.

48. The method of Claim 42, wherein the step of
regenerating comprises:

detecting added and missing synchronization pulses
in the modified synchronization signal;

modifying any detected added synchronization
pulses so they are no longer effective as
synchronization pulses; and

adding synchronization pulses at a location of any
detected missing synchronization pulses.

49. An apparatus for defeating a component video
protection signal which modifies a synchronization signal of
the component video to inhibit conversion thereof to a
composite video, comprising:

a terminal for receiving the modified
synchronization signal;

a circuit for regenerating the modified
synchronization signal to remove the modification; and

an output terminal for outputting the regenerated
synchronization signal.

50. The apparatus of Claim 49, wherein the circuit
generates a normal horizontal synchronization signal from a
vertical synchronization signal in the component video
signal.

51. The apparatus of Claim 50, wherein the circuit
includes:

an edge detector coupled to receive the vertical
synchronization signal;

a phase lock loop driven by an output signal from the edge detector; and

a one-shot circuit driven by the phase lock loop.

5 52. The apparatus of Claim 49, wherein the circuit includes:

a non-retriggerable one-shot circuit driven by a horizontal synchronization signal in the component video; and

10 a ringing circuit driven by an output signal of the one-shot circuit.

53. The apparatus of Claim 49, wherein the circuit includes:

15 a non-retriggerable one shot circuit driven by the synchronization signal in the component video; and
an oscillator driven by an output signal of the one shot circuit.

20 54. The apparatus of Claim 49, wherein the circuit includes:

a phase lock loop driven by the modified synchronization signal; and
a one shot circuit driven by the phase lock loop.

25 55. The apparatus of Claim 49, wherein the circuit includes:

a detector coupled to receive the modified synchronization signal and to detect added or deleted synchronization pulses;

30 a modifier coupled to the detector for modifying any detected added synchronization pulses so they are no longer effective as synchronization pulses; and

35 an adder coupled to the detector for adding synchronization pulses at a location of any detected missing synchronization pulses.

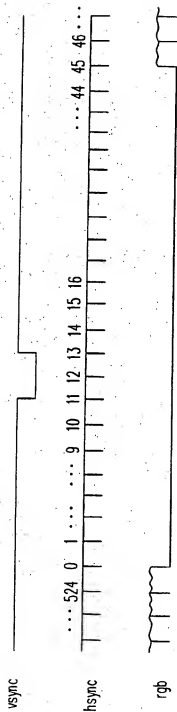


FIG. 1

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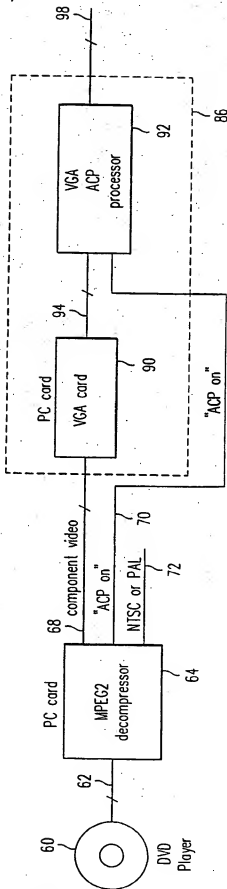
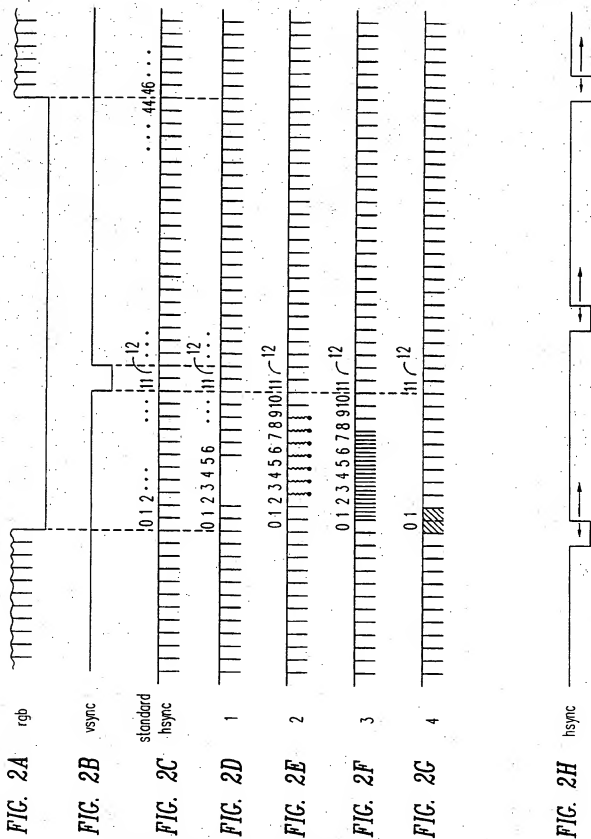


FIG. 3

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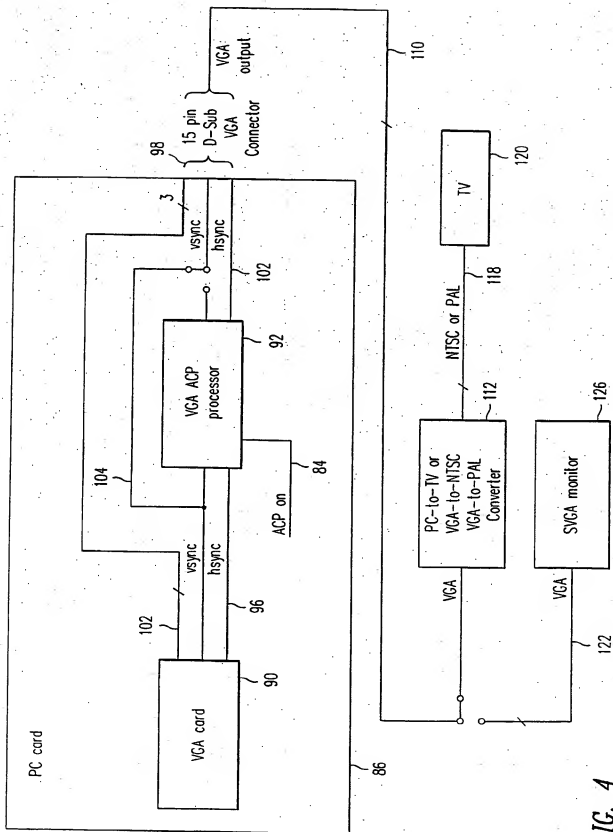
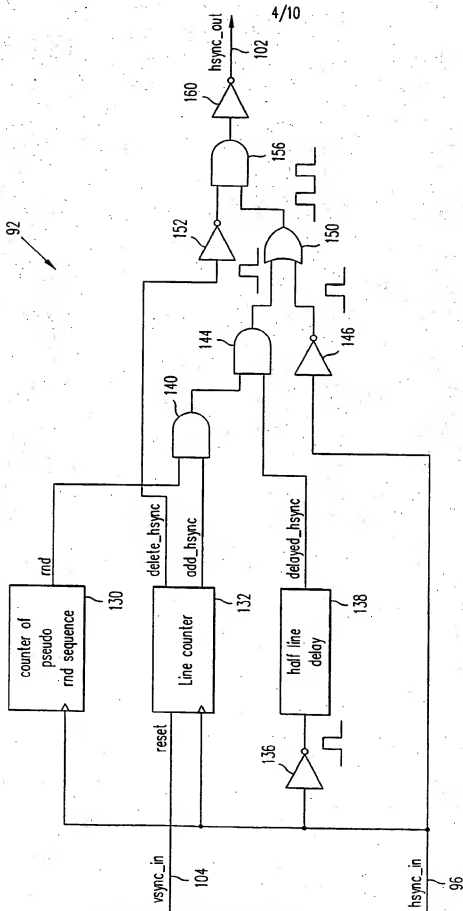


FIG. 4



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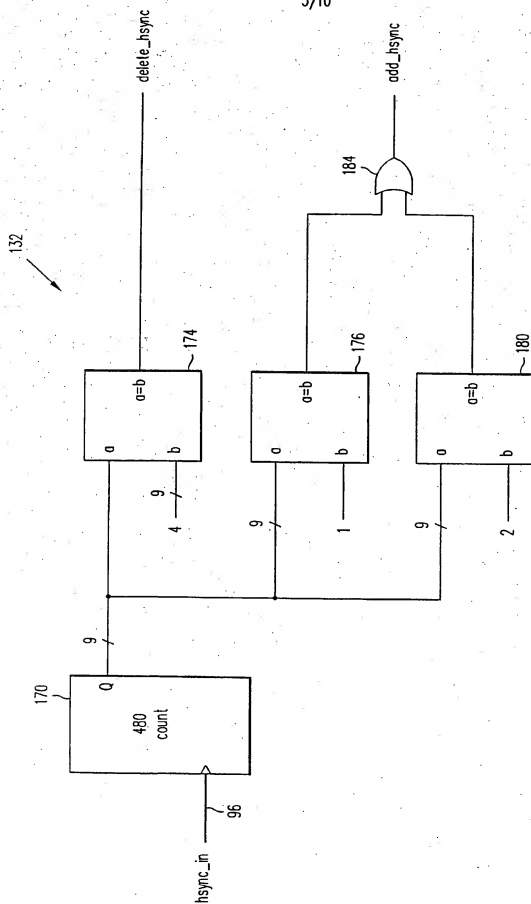


FIG. 6

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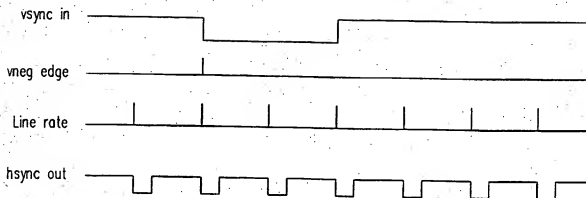


FIG. 7A

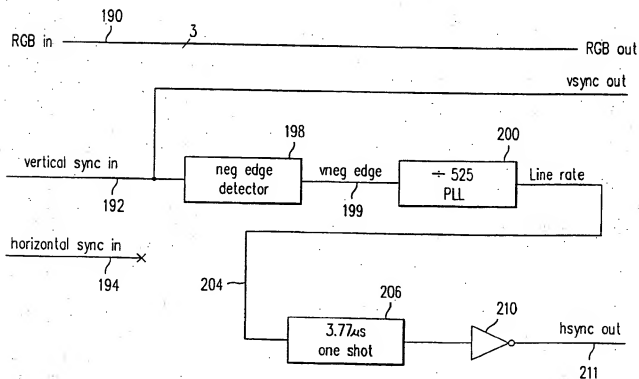
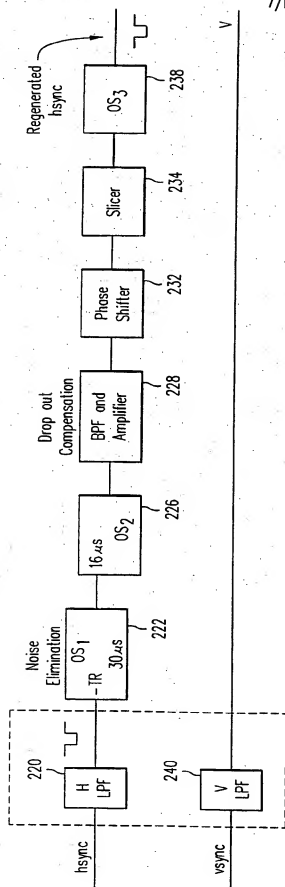


FIG. 7B

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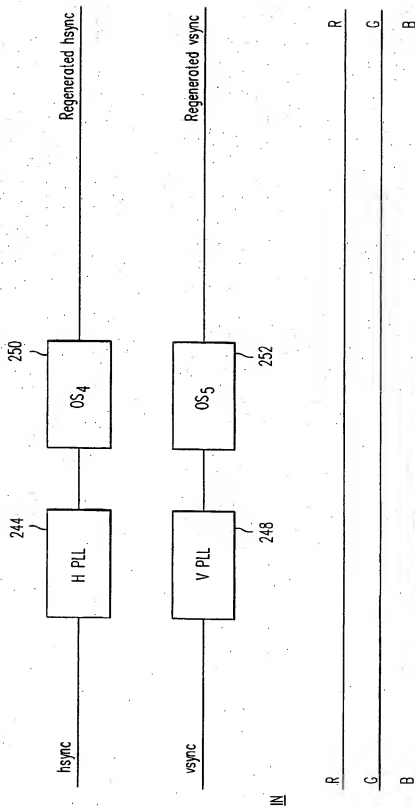


III

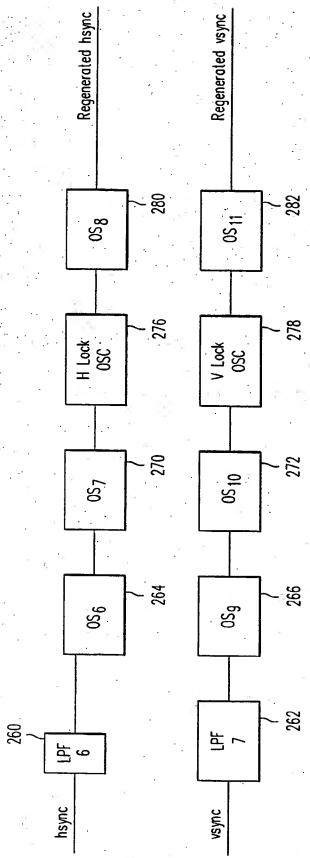
R	R
G	G
B	B

FIG. 8

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**FIG. 9**

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R	R
G	G
B	B

FIG. 10

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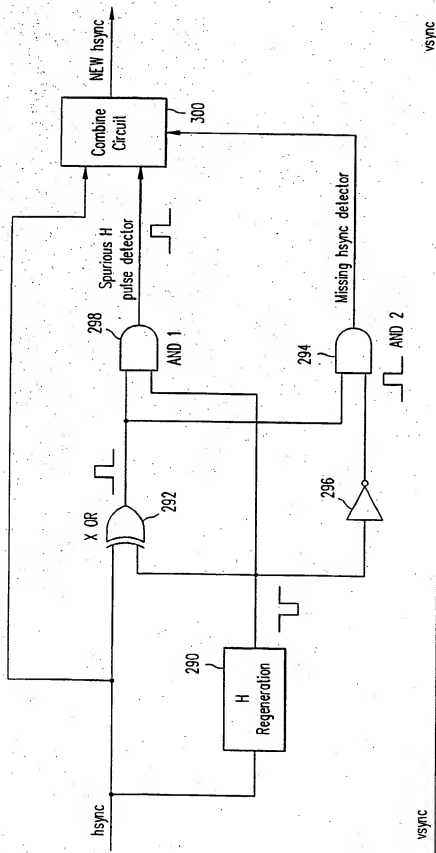


FIG. 11

INTERNATIONAL SEARCH REPORT

National Application No
PCT/US 98/12558

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04N5/913 H04N7/171

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 97.15142 A (MACROVISION CORP) 24 April 1997 see page 7, column 29, line 14 - page 34 see figures 1-9 ---	1, 3-21, 23-55
A	WO 94.24828 A (EIDAK CORP) 27 October 1994 see page 4, column 35, line 11 - page 2 see figures 2-4 -----	1, 3, 4, 6-12, 21, 23, 24, 26-32, 34, 35, 42, 43, 49

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Date of the actual completion of the international search

23 September 1998

Date of mailing of the international search report

06/10/1998

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European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Van der Zaal, R

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No.

PCT/US 98/12558

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9715142 A	24-04-1997	AU 7458096 A AU 7718396 A EP 0856224 A WO 9716022 A	07-05-1997 15-05-1997 05-08-1998 01-05-1997
WO 9424828 A	27-10-1994	US 5394470 A AU 6638294 A	28-02-1995 08-11-1994

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